DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings were received on 11 January 2008. These drawings are acceptable.

3. The drawings have not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the figures.

Specification

4. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-7 are rejected under 35 U.S.C. 102(e) as being anticipated by ***Hashimoto (US 7,046,223 B2)***.

Regarding claim 1, Hashimoto discloses a line inversion drive device [Fig. 1; circuits 32 and 50 operating in conjunction] (see Column 13, Lines 23-25) for a thin film transistor liquid crystal display [Figs. 1 & 20; 1] (see Column 1, Lines 25-27 & Column 15, Lines 55-58), comprising: a data inversion circuit [Fig. 2; circuits 33, 35, & 37 operating in conjunction], embedded in (i.e., incorporated with; fixed to; caused to be a part of; attached to) a clock [Fig. 1; e.g., DCLK, STH, & STV are all clock signals] controller [Fig. 1; circuits 6, 32, & 50 operating in conjunction], for receiving a data signal [Fig. 2; POL -- wherein this signal transmits information/data], said data inversion circuit, responsive to an inversion control signal [Fig. 2; STB, which is itself further responsive to Fig. 1's signal S_H] (see Column 1, Line 59 - Column 2, Line 14), determining whether to invert [Fig. 7; S_{SWN} -- wherein it is noted S_{SWN} is an polarity inverted version of signal POL] said data signal (see again Fig. 7; wherein it is further noted that signal POL itself alternates/inverts in polarity in synchronism with pulse STB) and outputting a display signal [Fig. 4; $V_{1\text{-}64}$] (see Column 19, Lines 8-39).

Regarding claim 2, Hashimoto discloses a line inversion drive circuit [Fig. 1; circuits 32 and 50 operating in conjunction] (see Column 13, Lines 23-25) for a thin film transistor liquid crystal display [Figs. 1 & 20; 1] (see Column 1, Lines 25-27 & Column 15, Lines 55-58),

comprising: a clock [Fig. 1; e.g., DCLK, STH, & STV are all clock signals] controller [Fig. 1; circuits 6, 32, & 50 operating in conjunction] including a data inversion circuit [Fig. 2; circuits 33, 35, & 37 operating in conjunction] for receiving a data signal [Fig. 2; POL] and a clock control device [Fig. 1; 50], said data inversion circuit being coupled to said clock control device (see Figs 1 & 2), said data inversion circuit responsive to an inversion control signal [Fig. 2; STB, which is itself further responsive to Fig. 1's signal S_H] (see Column 1, Line 59 - Column 2, Line 14) determining whether to invert [Fig. 7; S_{SWN} -- wherein it is noted S_{SWN} is an polarity inverted version of signal POL] said data signal (see again Fig. 7; wherein it is further noted that signal POL itself alternates/inverts in polarity in synchronism with pulse STB) and outputting a display signal [Fig. 4; V_{1-64}] (see Column 19, Lines 8-39); and a data line driver [Fig. 2; circuits 19 & 35-37 operating in conjunction], coupled to said data inversion device, for receiving a group of reference voltages [Figs. 2 & 4; V_{I1}~V_{I5}] (see Column 18, Lines 21-50), said data line driver, responsive to said group of reference voltages and said display signal, driving a plurality of data lines [Fig. 2; S_1-S_{528}] of said thin film transistor liquid crystal display (see Column 21, Lines 42-51).

Regarding claim 3, Hashimoto discloses a Gamma compensation circuit [Fig. 4; 35 and Fig. 5; 19] coupled to said data line driver to compensate (via both the "variation correcting mode" and the amplification circuitry) said display signal (see Column 2, Lines 56-60; Column 18, Lines 21-50; and Column 19, Line 40 - Column 20, Line 24).

Regarding claim 4, Hashimoto discloses a line inversion drive circuit [Fig. 1; circuits 32 and 50 operating in conjunction] (see Column 13, Lines 23-25) for a thin film transistor liquid crystal display [Figs. 1 & 20; 1] (see Column 1, Lines 25-27 & Column 15, Lines 55-58), comprising: a clock [Fig. 1; e.g., DCLK, STH, & STV are all clock signals] controller [Fig. 1; circuits 6, 32, & 50 operating in conjunction] including a data inversion circuit [Fig. 2; circuits 33, 35, & 37 operating in conjunction] for receiving a data signal [Fig. 2; POL], the clock controller for generating an inversion control signal [Fig. 2; STB, which is itself generated via Fig. 1's signal S_H] (see Column 1, Line 59 - Column 2, Line 14) to said data inversion circuit to determine whether to invert [Fig. 7; S_{SWN} -- wherein it is noted S_{SWN} is an polarity inverted version of signal POL] said data signal (see again Fig. 7; wherein it is further noted that signal POL itself alternates/inverts in polarity in synchronism with pulse STB), said data inversion circuit, responsive to said inversion control signal, outputting a display signal [Fig. 4; $V_{1\text{-}64}$] (see Column 19, Lines 8-39); and a data line driver [Fig. 2; circuits 19 & 35-37 operating in conjunction], coupled to said data inversion circuit, for receiving a group of reference voltages [Figs. 2 & 4; V_{I1}~V_{I5}] (see Column 18, Lines 21-50), said data line driver, responsive to said group of reference voltages and said display signal, driving a plurality of data lines [Fig. 2; S_1-S_{528}] of said thin film transistor liquid crystal display (see Column 21, Lines 42-51).

Regarding claim 5, Hashimoto discloses a line inversion drive device [Fig. 1; circuits 32 and 50 operating in conjunction] (see Column 13, Lines 23-25) for a thin film transistor liquid crystal display [Figs. 1 & 20; 1] (see Column 1, Lines 25-27 & Column 15, Lines 55-58), comprising: a clock [Fig. 1; e.g., DCLK, STH, & STV are all clock signals] controller [Fig. 1;

circuits 6, 32, & 50 operating in conjunction] including a data inversion circuit [Fig. 2; circuits 33, 35, & 37 operating in conjunction] for receiving a data signal [Fig. 2; POL], the clock controller for generating an inversion control signal [Fig. 2; STB, which is itself generated via Fig. 1's signal S_H] (see Column 1, Line 59 - Column 2, Line 14) to said data inversion circuit to determine whether to invert [Fig. 7; S_{SWN} -- wherein it is noted S_{SWN} is an polarity inverted version of signal POL] said data signal (see again Fig. 7; wherein it is further noted that signal POL itself alternates/inverts in polarity in synchronism with pulse STB), said data inversion circuit, responsive to said inversion control signal, outputting a display signal [Fig. 4; V_{1-64}] (see Column 19, Lines 8-39).

Regarding claim 6, Hashimoto discloses a line inversion drive method [Fig. 1; via circuits 32 and 50 operating in conjunction] (see Column 13, Lines 23-25) for a thin film transistor liquid crystal display [Figs. 1 & 20; 1] (see Column 1, Lines 25-27 & Column 15, Lines 55-58) to drive a plurality of data lines [Fig. 2; S_1-S_{528}], comprising the steps of: receiving an input signal [Fig. 2; POL] and a group of reference voltages [Figs. 2 & 4; V_{I1}~V_{I5}] (see Column 18, Lines 21-50); determining whether to invert [Fig. 7; S_{SWN} -- wherein it is noted S_{SWN} is an polarity inverted version of signal POL] said input signal (see again Fig. 7; wherein it is further noted that signal POL itself alternates/inverts in polarity in synchronism with pulse STB), responsive to an inversion control signal [Fig. 2; STB, which is itself responsive to Fig. 1's signal S_H] (see Column 1, Line 59 - Column 2, Line 14), and output a display signal [Fig. 4; V_{1-64}] (see Column 19, Lines 8-39); compensating [via Fig. 4; 35 and Fig. 5; 19] said display signal; and driving said plurality of data lines responsive (via both the "variation correcting mode" and the amplification

circuitry) to said compensated display signal and said group of reference voltages (see Column 2, Lines 56-60; Column 18, Lines 21-50; and Column 19, Line 40 - Column 20, Line 24).

Regarding claim 7, Hashimoto discloses said step of compensating said display signal is performed by Gamma compensation (see Column 2, Lines 56-60).

Response to Arguments

7. Applicant's arguments filed 11 January 2008 have been fully considered but they are not persuasive.

The Applicant contends, "*the circuits 33, 35 and 37 shown in FIG. 2 of Hashimoto operate in conjunction with the data inversion circuit of the present application as presented in page 10, line 2 of the current Office Action. However, Applicants understand that said assertion is not accurate, because the circuits 33, 35 and 37 are not embedded in the control circuit 50, while the data inversion circuit of the present invention is embedded in the dock controller. As such, Hashimoto fails to disclose, teach or suggest at least the feature [of a data inversion circuit, embedded in a clock controller]*" (see Page 18 of the Amendment filed 11 January 2008). However, the examiner respectfully disagrees.

Hashimoto discloses a data inversion circuit [Fig. 2; circuits 33, 35, & 37 operating in conjunction], embedded in (i.e., *incorporated with; fixed to; caused to be a part of; attached to*) a clock [Fig. 1; DCLK, STH, & STV and Fig. 4; CLK are all clock signals] controller [Fig. 1; circuits 6, 32, & 50 operating in conjunction] (see Column 1, Line 59 - Column 2, Line 14). The

circuitry illustrated in Figure 2 is "embedded in" the data electrode driving circuit 32 shown in Figure 1. Furthermore, taking the circuits [Fig. 2; 33, 35, & 37] as a communicatively coupled whole device (that is, image a boundary line surrounding circuits 33, 35, & 37) results in the circuitry illustrated in Figure 2 being "embedded in" the combined circuitry device [Fig. 2; 33 + 35 + 37].

The Applicant also contends, " '*polarity signal POL is a signal that inverts in every one horizontal sync period' as recited in column 2, lines 10-11 and 'the strobe signal STB is a signal having a same period as that of the horizontal sync signal* S_H*' as recited in column 1, lines 66 to column 2, line 1. It is deduced from the above comparison that POL is not the data signal and STB is not the inversion control signal. Thus, the data inversion circuit is not to invert data signal and output the display signal according to STB*" (see Page 18 of the Amendment filed 11 January 2008). However, the examiner again respectfully disagrees.

Hashimoto discloses receiving a data signal [Fig. 2; POL -- wherein this signal transmits information/data], said data inversion circuit, responsive to an inversion control signal [Fig. 2; STB, which is itself further responsive to Fig. 1's signal S_H] (see Column 1, Line 59 - Column 2, Line 14), determining whether to invert [Fig. 7; S_{SWN} -- wherein it is noted S_{SWN} is an polarity inverted version of signal POL] said data signal (see again Fig. 7; wherein it is further noted that signal POL itself alternates/inverts in polarity in synchronism with pulse STB) and outputting a display signal [Fig. 4; V_{1-64}] (see Column 19, Lines 8-39).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., *a data signal*

providing video image pixel values) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Lastly, The Applicant contends, "*In accordance with the currently amended claim 6, the input signal is inverted firstly to output the display signal, and then the display signal is compensated. However, in Hashimoto, the display signal is compensated firstly, and then the input signal is inverted to output the display signal. Thus, the operation mode of the present application is different from that of Hashimoto*" (see Page 19 of the Amendment filed 11 January 2008). However, the examiner respectfully disagrees.

Hashimoto discloses receiving an input signal [Fig. 2; POL] and a group of reference voltages [Figs. 2 & 4; V_{I1}~V_{I5}] (see Column 18, Lines 21-50); determining whether to invert [Fig. 7; S_{SWN} -- wherein it is noted S_{SWN} is an polarity inverted version of signal POL] said input signal (see again Fig. 7; wherein it is further noted that signal POL itself alternates/inverts in polarity in synchronism with pulse STB), responsive to an inversion control signal [Fig. 2; STB, which is itself responsive to Fig. 1's signal S_H] (see Column 1, Line 59 - Column 2, Line 14), and output a display signal [Fig. 4; V_{1-64}] (see Column 19, Lines 8-39).

Hashimoto also discloses compensating [via Fig. 4; 35 and Fig. 5; 19] said display signal; and driving said plurality of data lines responsive (via both the "variation correcting mode" and the amplification circuitry) to said compensated display signal and said group of reference voltages (see Column 2, Lines 56-60; Column 18, Lines 21-50; and Column 19, Line 40 - Column 20, Line 24).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., *that the claimed steps must occur in a specific chronological order; that the steps cannot occur simultaneously; and/or that one step must fully complete before the next step begins*) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

By such reasoning, rejection of the claims is deemed necessary, proper, and thereby maintained at this time.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Piziali/
Primary Examiner, Art Unit 2629
9 April 2008